Microburst
Development System

General Description

The Microburst Development System is a companion development platform for the Microburst SDR. Waveforms developed on the Microburst Development System port directly to Microburst SDR. The development system offers multiple debug test points for development. The Microburst Development System is a full duplex COTS solution providing signal communications systems engineers and waveform developers with a fully functional, reconfigurable radio development platform. The direct conversion architecture provides continuous RF coverage over the full operating range.

The configuration includes a full-duplex RF transceiver, a consolidated digital system with the TI OMAP 37x GPP/DSP processor + Xilinx Spartan-6 FPGA, and a wide-band RF front end module, all operating in an open source Linux-based environment and enclosed in a 1U housing.

Benefits

- Reduces cost and time-to-market
- Wide RF operating range:
  30 MHz to 3800 MHz
- Frequency covers a variety of wireless protocol applications– UHF, White Space, WiFi, WiMax, LTE
- Enables SDR development on OMAP platform
- OMAP platform supports development of waveforms and applications on Linux, VxWorks, or Android Operating Systems
- Includes fast-start templates, reference waveform implementation; tool suite and support packages available
- Rugged 1U enclosure with removable cover for access to the hardware

Applications

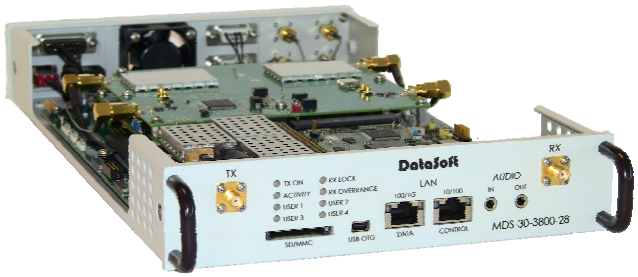
- Commercial PHY-MAC waveform and applications development
- Cognitive and spectrally fragmented waveform development
- Networked and spectrum agile waveform development
- Whitespace and Dynamic Spectrum Access Research

RF System Features

- Full-duplex (FDD, TDD) transceiver architecture with programmable signal bandwidths from 1.5 MHz to 28 MHz
- Continuous RF transceiver frequency coverage from 30 MHz to 3800 MHz (FEM dependent)
- 12-bit Dual-channel DAC and ADC at 40 Msps
- Direct Conversion Architecture
- Front End Module (FEM) covering multiple frequency options for low noise amplification, output power amplification and preselect filtering

Digital System Features

- Low cost baseband platform based on TI's OMAP 37x multimedia applications processor
- Advanced Superscaler ARM© Cortex™ RISC core with a C64x+ DSP core
- Multiple data and user interfaces
- Integrated GPS receiver with accurate 1-PPS output



Microburst Development System
Waveform and algorithm development platform for Microburst SDR

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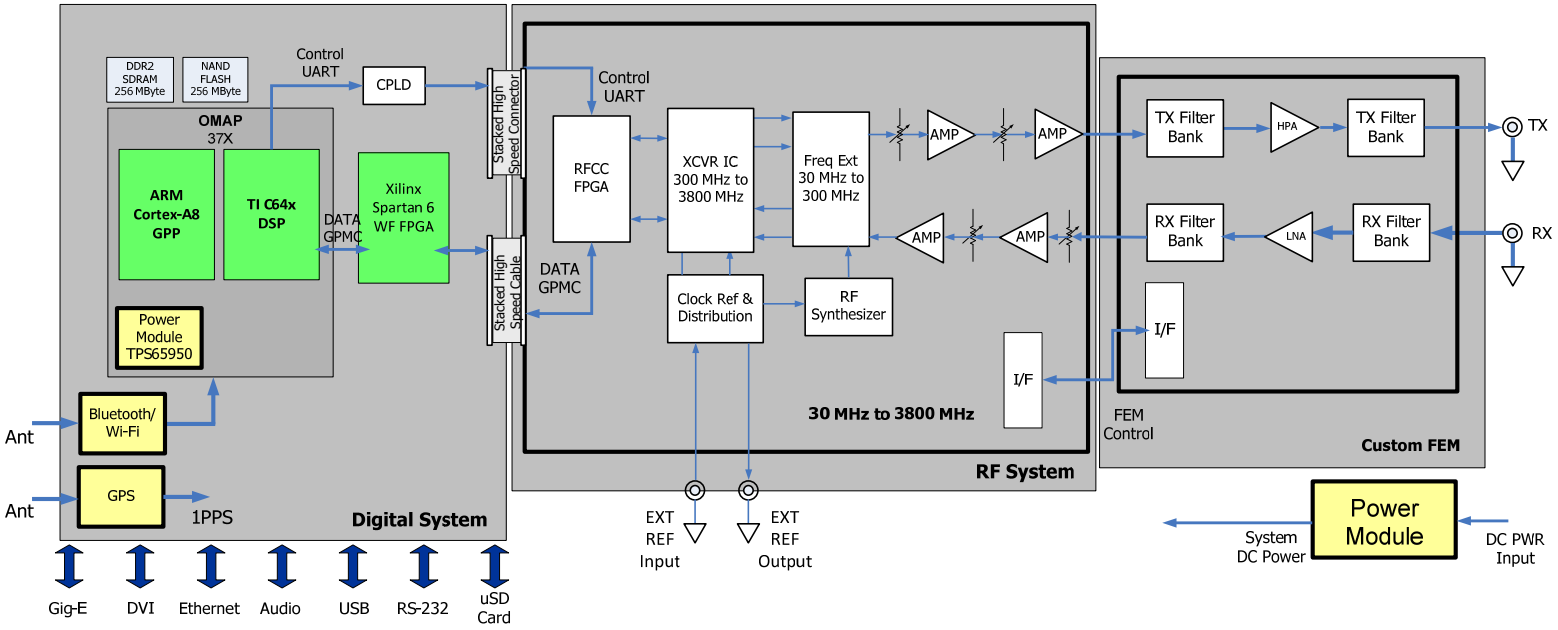
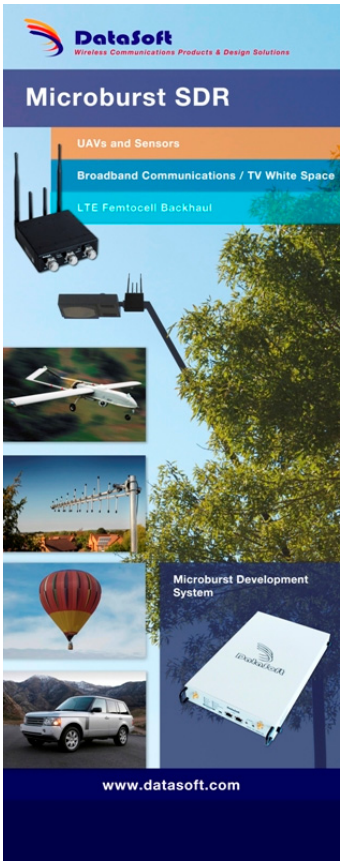
Microburst Development System Block Diagram





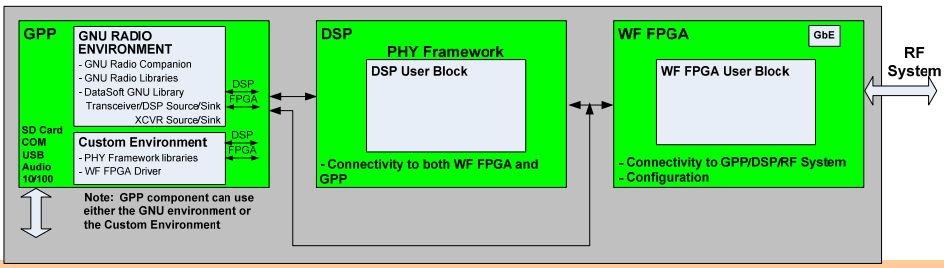
The Microburst SDR and SDR Development System are based on the Texas Instruments OMAP processor family, the Xilinx Spartan-6 FPGA platform, commercial Wi-Fi/Bluetooth/GPS ICs, and a flexible RF transceiver for industrial, consumer, and telecommunications radio applications

- *LTE Femtocell Backhaul*
- *Broadband Communications*
- *Remote Sensing/Surveying*

Microburst
Development System

DataSoft

Microburst Development System Processor Framework



	GPP	DSP	FPGA
	DM3730 ARM Cortex-A8 1 GHz	**DM3730 C64x+ 800 MHz**	**Spartan-6 LX75 or LX150**
Target: Provided with Microburst			
Operating System	Arago Linux 2.6.32 Kernel	DSP/Bios	
Toolchain	Mentor Graphics Sourcery G++ Lite	TMS320C6000 C/C++ Code Generation Tools	LX75—Xilinx ISE WebPack (Free FPGA Development Tools) LX150—Xilinx ISE tools required
Load Mechanism	• **Boot loaders and kernel** load from SD card • **Root Filesystem** mounts from SD card or NFS	Loaded from GPP with TI DSP/ Bios DSPLink interface	Loaded by GPP with Microburst driver
Developers Kit	• Microburst drivers for transceiver control and data communication • Sample applications to demonstrate interfaces • Microburst PSP with drivers for Ethernet, audio, UART, USB, MMC/SD interfaces • Control Panel HTTP GUI • GNU Radio FM, DQPSK demo apps with Microburst interface blocks	• Microburst drivers for transceiver data communication • Sample applications to demonstrate interfaces • Based on DSP/BIOS and DSPLink	• ISE project with source code for WF FPGA project including dedicated User Block for custom applications • Basic FPGA framework and data path connectivity • 16 user-defined D/A converter probe points (requires DAC accessory) • Rear panel user-defined GPIOs
Additional Tools	TI DVSDK with array of ARM tools	TI DVSDK with array of DSP tools	
Host Development Environment: Provided with Microburst (or free download with instructions in documentation)			
Operating System	Ubuntu 10.04 LTS; Virtual Machine included	• Ubuntu 10.04 LTS • Windows for CCS 4.X	Windows or Linux
Connectivity	Tera Term or any terminal program		
Available Development Tools: User must purchase			
IDE	Any Linux IDE	TI Code Composer Studio	
Emulator/Debug	GDB	Spectrum Digital XDS510USB Plus	Xilinx Platform Cable USB II Probe
Packages	Wide range of open source software can be cross compiled for Microburst	TI and third party C64x+ components	Xilinx and third party FPGA cores

GPP, DSP, and FPGA resources are available for maximum design flexibility

Basic infrastructure and connectivity are in place for processing elements to jumpstart waveform development

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Microburst
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Preliminary Specifications

Overall

Full Duplex Symbol Rates	up to 10 Msym/s
Frequency Stability	± 2.5 ppm
Operating Temperature Range	0 ° to +50° C
Storage Temperature Range	-40° to +85° C
Size	13.25" x 8" x 1.75"
Weight	< 4 lb
Power Consumption	TBD

Transmitter

Output Impedance	50 ohms
Output Return Loss	10 dB
Frequency Range (FEM dependent)	30 MHz to 3800 MHz
Frequency Resolution	2.4 Hz
TX Variable Output Power	2 Watts
Output Power Step Size	1 dB
Output Power Accuracy	± 1 dB
P1dB	TBD
Output IP3	TBD
SSB Phase Noise: (Offset from Fcenter = 1000 MHz)	
100 Hz	-95 dBc/Hz
1 KHz	-110 dBc/Hz
10 KHz	-121 dBc/Hz
100 KHz	-115 dBc/Hz
10 MHz	-135 dBc/Hz
Programmable Signal Bandwidth (RF)	1.5 MHz to 28 MHz
Carrier Feedthrough	TBD
Sideband Suppression	TBD
Max DAC Sample Rate (12-bit)	40 Msps

Receiver

Input Impedance (nominal)	50 ohms
Input Return Loss	10 dB
Frequency Range (FEM dependent)	30 MHz to 3800 MHz
Frequency Resolution	2.4 Hz
Noise Figure	< 10 dB (FEM dependent)
Maximum Composite Input Power	+ 25 dBm
Expected Input Power	TBD
Input IP3	TBD
SSB Phase Noise: (Offset from Fcenter = 1000 MHz)	
100 Hz	-95 dBc/Hz
1 KHz	-110 dBc/Hz
10 KHz	-121 dBc/Hz
100 KHz	-115 dBc/Hz
10 MHz	-135 dBc/Hz
Programmable Signal Bandwidth (RF)	1.5 MHz to 28 MHz
Baseband Gain	+ 40 dB
Sensitivity (1.5 MHz)	TBD
Max ADC Sample Rate (12-bit)	40 Msps

Wi-Fi/Bluetooth

Wireless Standard	2.4 GHz IEEE 802.11 b/g/n; Bluetooth 2.1 + EDR, Power Class 1.5
WLAN RF Frequency Range	2.412 GHz to 2.472 GHz
Bluetooth RF Frequency Range	2.402 GHz to 2.480 GHz

The specifications listed are engineering estimates that are believed to be accurate and reliable.
The information is subject to change without notice.

Included Software and Documentation

- Embedded Arago Linux Kernel from TI with Device Drivers for: UART, Sound Device, SD Card and Ethernet
- Software Development Kit (SDK)
  - Source Code for: U-Boot, GNU Radio, RF Device Drivers, GNU Radio RF Blocks, SDR System Control Panel
  - Root File System containing all precompiled source code
- Development environment WF implementations with customization available
- Supported Software Loading Environments:
  - Standalone (NAND+SD Card)
  - Network (NAND+TFTP or NAND+NFS)
- Fast-start templates and example waveforms

DataSoft was founded in 1995 and has operations in Tempe, AZ.

For additional information, visit our web site at www.datasoft.com or email sales@datasoft.com.